Jameco Part number 148427

P/N 148435
P/N 148427

MOSEL VITELIC ***V53C16258H*** ***PRELIMINARY***

HIGH PERFORMANCE
256K X 16 EDO PAGE MODE
CMOS DYNAMIC RAM
OPTIONAL SELF REFRESH

HIGH PERFORMANCE	**30**	**35**	**40**	**45**	**50**
Max. $\overline{RAS}$ Access Time, (t_{RAC})	30 ns	35 ns	40 ns	45 ns	50 ns
Max. Column Address Access Time, (t_{CAA})	16 ns	18 ns	20 ns	22 ns	24 ns
Min. Extended Data Out Mode Cycle Time, (t_{PC})	12 ns	14 ns	15 ns	17 ns	19 ns
Min. Read/Write Cycle Time, (t_{RC})	65 ns	70 ns	75 ns	80 ns	90 ns

Features

- 256K x 16-bit organization
- EDO Page Mode for a sustained data rate of 83 MHz
- RAS access time: 30, 35, 40, 45, 50 ns
- Dual CAS Inputs
- Low power dissipation
- Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh
- Optional Self Refresh (V53C16258SH)
- Refresh Interval: 512 cycles/8 ms
- Available in 40-pin 400 mil SOJ and 40/44L-pin 400 mil TSOP-II packages
- Single +5V ±10% Power Supply
- TTL Interface

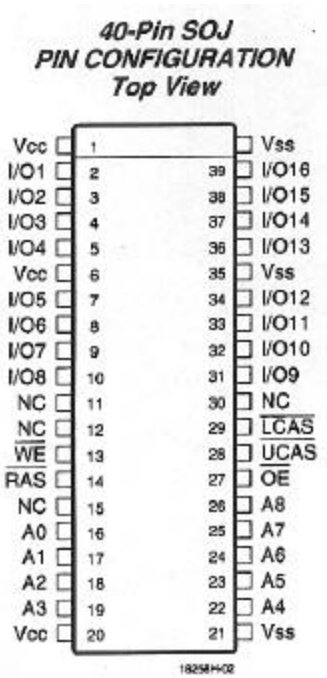
Description

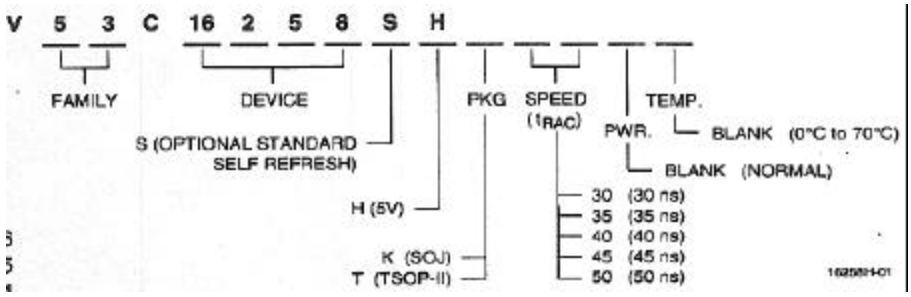
The V53C16258H is a high speed 262, 144 x 16 bit high performance CMOS dynamic random access memory. The V53C16258H offers a combination of unique features including: EDO Page Mode operation for higher sustained bandwidth with Page Mode cycle times as short as 12ns. All inputs are TTL compatible. Input and output capicatance is significantly lowered to increase performance and minimize loading. These features make the V53C16258H ideally suited for a wide variety of high performance computer systems and peripheral applications.

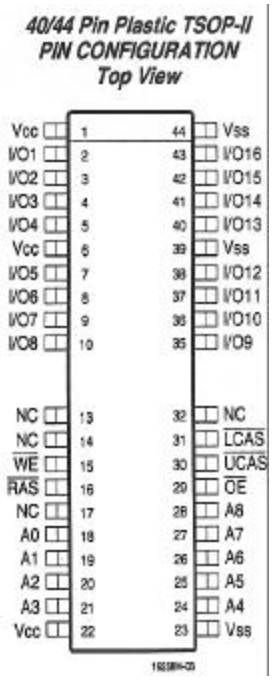
Device Usage Chart

Operating Temperature Range	**Package Outline**		**Access Time (ns)**					**Power**	**Temperature Mark**
	K	**T**	**30**	**35**	**40**	**45**	**50**	**Std.**	
0°C to 70°C	·	·	·	·	·	·	·	·	Blank

Part Name	Self Refresh	Supply Voltage	Package	Speed
V53C16258HKxx	No Self Refresh	5V	SOJ	30/35/40/45/50
V53C16258HTxx	No Self Refresh	5V	TSOP	30/35/40/45/50
V53C16258SHKxx	Optional Standard Self Refresh (8ms)	5V	SOJ	30/35/40/45/50
V53C16258SHTxx	Optional Standard Self Refresh (8ms)	5V	TSOP	30/35/40/45/50







Pin Names

A_0-A_8	Address Inputs
RAS	Row Address Strobe
UCAS	Column Address Strobe/Upper Byte Control
LCAS	Column Address Strobe/Lower Byte Control
WE	Write Enable
OE	Output Enable
I/O_1-I/O_{16}	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias..…… -10°C to +80°C
Storage Temperature (plastic)……. -55°C to +125°C
Voltage Relative to V_{SS}..... -1.0 V to +7.0 V
Data Output Current……..…50 mA
Power Dissipation…….……1.0 W

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

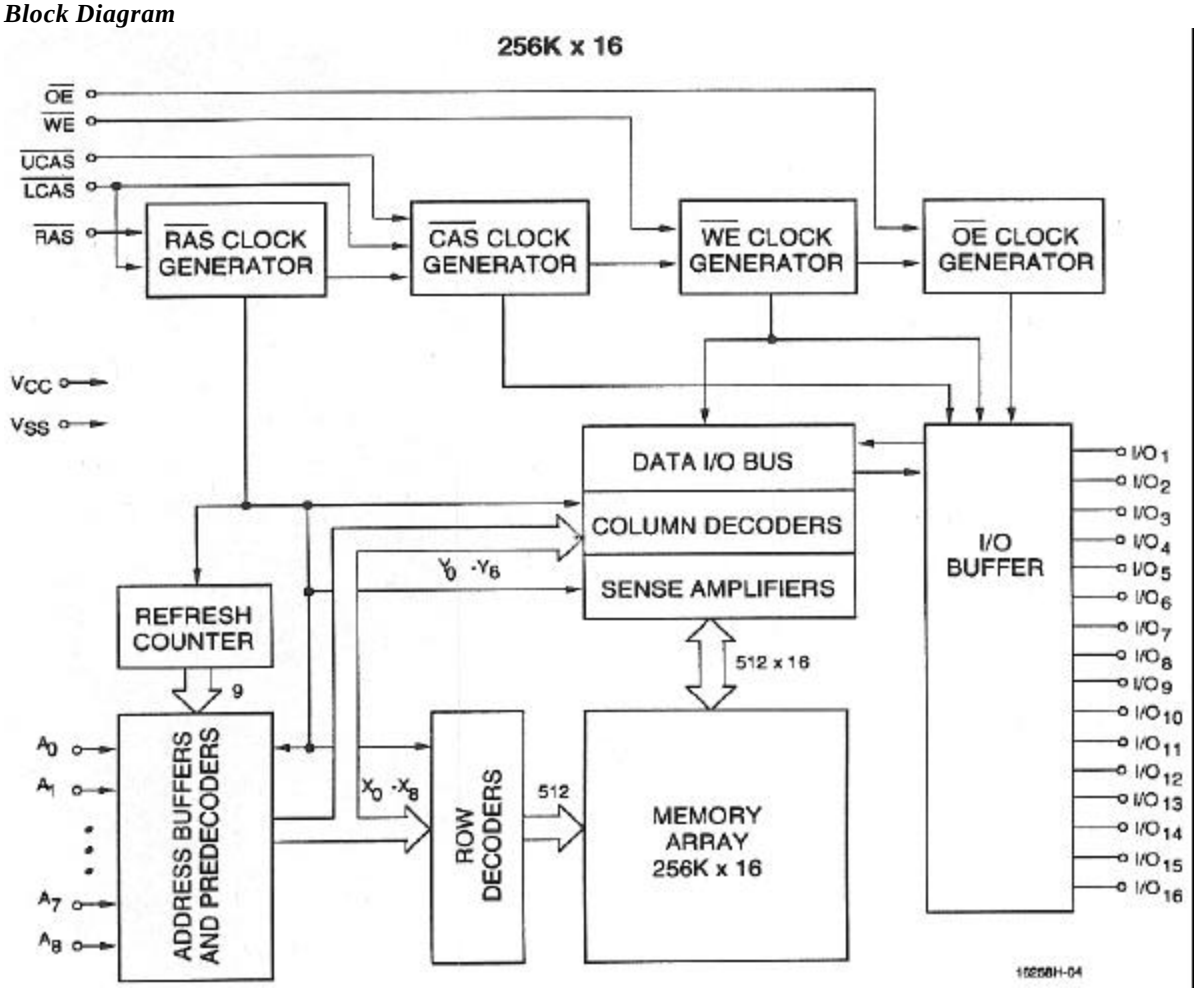
Capacitance*

T_A = 25°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	RAS, CAS, WE, OE 4	5	pF	
C_{OUT}	Data Input/Output	5	7	pF

***Note:** Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

			V53C16258H					
Symbol	**Parameter**	**Access Time**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**	**Notes**
I_{LI}	Input Leakage Current (any input pin)		-10		10	Ì A	$V_{SS} \le V_{IN} \le V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-10		10	Ì A	$V_{SS} \le V_{OUT} \le V_{CC}$ RAS, CAS at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	30			200	MA	$t_{RC} = t_{RC}$ (min.)	1, 2
		35			190			
		40			180			
		45			170			
		50			160			
I_{CC2}	V_{CC} Supply Current, TTL Standby				2	MA	RAS, CAS at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, RAS-Only Refresh	30			200	MA	$t_{RC} = t_{RC}$ (min.)	2
		35			190			
		40			180			
		45			170			
		50			160			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	30			190	mA	Minimum Cycle	1, 2
		35			180			
		40			180			
		45			160			
		50			150			
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled other inputs ≥ V_{SS}				2	mA	RAS = V_{IH}, CAS = V_{IL}	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				1	mA	RAS ≥ V_{CC} - 0.2 V, CAS ≥ V_{CC} - 0.2 V, All other inputs ≥ V_{SS}	
I_{CC7}	Self Refresh Current				400	ì A	CBR Cycle with t_{RAS} ≥ t_{RASS} (Min.) and CAS = V_{IL}; WE = V_{CC}-0.2V; A_0-A_8 and D_{IN} = V_{CC}-0.2V	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{CC} + 1	V		3
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2 Ma	
V_{OH}	Output High Voltage		2.4			V	I_{OH} = -2 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0V unless otherwise noted AC Test conditions, input pulse levels 0 to 3V

			30		35		40		45		50			
#	Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Notes
1	T_{RAS}	RAS Pulse Width	30	75K	35	75K	40	75K	45	75K	50	75K	ns	
2	T_{RC}	Read or Write Cycle Time	65		70		75		80		90		ns	
3	T_{RP}	RAS Precharge Time	25		25		25		25		30		ns	
4	T_{CSH}	CAS Hold Time	30		35		40		45		50		ns	
5	T_{CAS}	CAS Pulse Width	5		6		7		8		9		ns	
6	T_{RCD}	RAS to CAS Delay	15	20	16	24	17	28	18	32	19	36	ns	
7	T_{RCS}	Read Command Setup Time	0		0		0		0		0		ns	4
8	T_{ASR}	Row Address Setup Time	0		0		0		0		0		ns	
9	T_{RAH}	Row Address Hold Time	5		6		7		8		9		ns	
10	T_{ASC}	Column Address Setup Time	0		0		0		0		0		ns	
11	T_{CAH}	Column Address Hold Time	5		5		5		6		7		ns	
12	$T_{RSH\ (R)}$	RAS Hold Time (Read Cycle)	10		10		10		10		10		ns	
13	T_{CRP}	CAS to RAS Precharge Time	5		5		5		5		5		ns	
14	T_{RCH}	Read Command Hold Time Referenced to CAS	0		0		0		0		0		ns	5
15	T_{RRH}	Read Command Hold Time Referenced to RAS	0		0		0		0		0		Ns	5
16	T_{ROH}	RAS Hold Time Referenced to OE	6		7		8		9		10		ns	
17	T_{OAC}	Access Time from OE		10		11		12		13		14	ns	12
18	T_{CAC}	Access Time from CAS		10		11		12		13		14	ns	6, 7, 14
19	T_{RAC}	Access Time from RAS		30		35		40		45		50	ns	6, 8, 9
20	T_{CAA}	Access Time from Column Address		16		18		20		22		24	ns	6, 7, 10
21	T_{LZ}	OE or CAS to Low-Z Output	0		0		0		0		0		ns	16
22	T_{HZ}	OE or CAS to High-Z Output	0	5	0	6	0	6	0	7	0	8	ns	16
23	T_{AR}	Column Address Hold Time from RAS	26		28		30		35		40		ns	
24	T_{RAD}	RAS to Column Address Delay Time	10	14	11	17	12	20	13	23	14	26	ns	11
25	$T_{RCH(w)}$	RAS or CAS Hold Time in Write Cycle	10		10		10		10		10		ns	
26	T_{CWL}	Write Command to CAS Lead Time	10		11		12		13		14		ns	
27	T_{WCS}	Write Command Setup Time	0		0		0		0		0		ns	12, 13
28	T_{WCH}	Write Command Hold Time	5		5		5		6		7		ns	

AC Characteristics

#	Symbol	Parameter	30		35		40		45		50		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
29	T_{WP}	Write Pulse Width	5		5		5		6		7		ns	
30	T_{WCR}	Write Command Hold Time from RAS	26		28		30		35		40		ns	
31	T_{RWL}	Write Command to RAS Lead Time	10		11		12		13		14		ns	
32	T_{Ds}	Data in Setup Time	0		0		0		0		0		ns	14
33	T_{DH}	Data in Hold Time	5		5		5		6		7		ns	14
34	T_{WOH}	Write to OE Hold Time	5		6		6		7		8		ns	14
35	T_{OED}	OE to Data Delay Time	5		5		6		7		8		ns	14
36	T_{RWC}	Read-Modify-Write Cycle Time	100		105		110		115		130		ns	
37	T_{RRW}	Read-Modify-Write Cycle RAS Pulse Width	65		70		75		80		87		ns	
38	T_{CWD}	CAS to WE Delay	26		28		30		32		34		ns	12
39	T_{RWD}	RAS to WE Delay in Read-Modify-Write Cycle	50		54		58		62		68		ns	12
40	T_{CRW}	CAS Pulse Width (RMW)	44		46		48		50		52		ns	
41	T_{AWD}	Col. Address to WE Delay	32		35		38		41		42		ns	12
42	T_{PC}	EDO Fast Page Mode Read or Write Cycle Time	12		14		15		17		19		ns	
43	T_{CP}	CAS Precharge Time	3		4		5		6		7		Ns	
44	T_{CAR}	Column Address to RAS Setup Time	16		18		20		22		24		ns	
45	T_{CAP}	Access Time from Column Precharge		19		21		23		25		27	ns	7
46	T_{DHR}	Data in Hold Time Referenced to RAS	26		28		30		35		40		ns	
47	T_{CSR}	CAS Setup Time CAS-before-RAS Refresh	10		10		10		10		10		ns	
48	T_{RPC}	RAS to CAS Precharge Time	0		0		0		0		0		ns	
49	T_{CHR}	CAS Hold Time CAS-before-RAS Refresh	7		8		8		10		12		ns	
50	T_{PCM}	EDO Page Mode Read-Modify-Write Cycle Time	56		58		60		65		70		ns	
51	T_{COH}	Output Hold After CAS Low	5		5		5		5		5		ns	
52	T_{OES}	OE Low to CAS High Setup Time	5		5		5		5		5		ns	
53	T_{OEH}	OE Hold Time from WE during Read-Modify Write Cycle	10		10		10		10		10		ns	
54	T_{OEP}	OE High Pulse Width	10		10		10		10		10		ns	

AC Characteristics

#	Symbol	Parameter	30		35		40		45		50		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
55	t_T	Transition Time (Rise and Fall)	1.5	50	1.5	50	1.5	50	1.5	50	1.5	50	ns	15
56	t_{REF}	Refresh Interval (512 Cycles)		8		8		8		8		8	ms	17
Optional Self Refresh														
57	t_{RASS}	RAS Pulse Width During Self Refresh	100		100		100		100		100		ìs	18
58	t_{RPS}	RAS Precharge Time During Self Refresh	100		100		100		100		100		ns	18
59	t_{CHS}	CAS Hold Time Width During Self Refresh	100		100		100		100		100		ns	18

Notes:

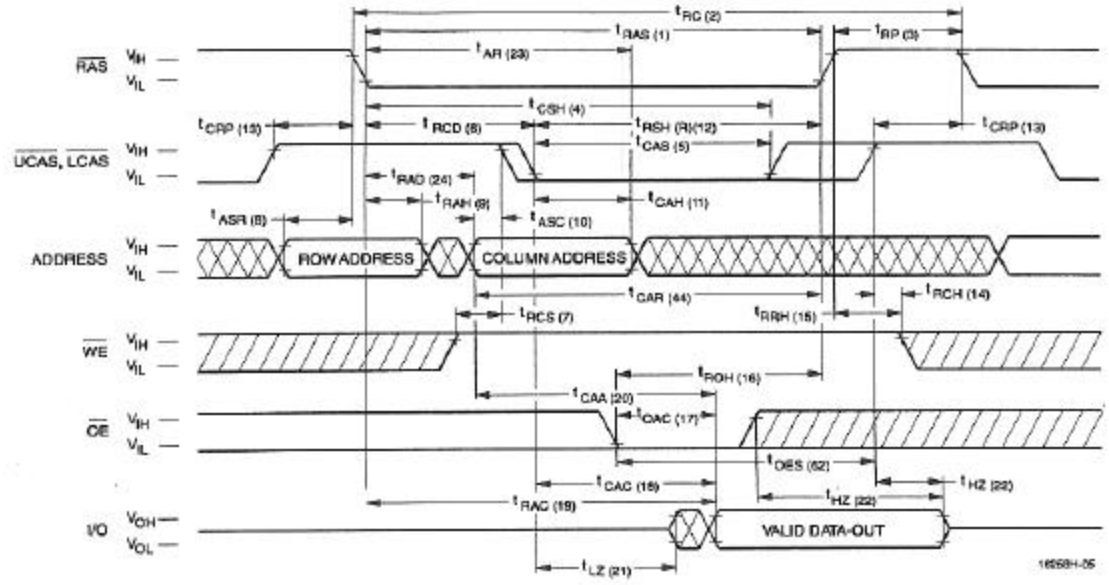
1. l_{CC} is dependent on output loading when the device output is selected. Specified l_{CC} (max.) is measured with the output open.
2. l_{CC} is dependent upon the number of address transitions. Specified l_{CC} (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to -1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{CC}
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL input and 50 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of CAS or WE.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T= 3ns.
16. Assumes a three-state test load (5 pF and a 500 Ohm Thevenin equivalent).
17. An initial 200 ìs pause and 8 RAS-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. One CBR refresh or complete set of row refreah cycles must be completed upon exiting Self Refreah Mode.

Truth Table

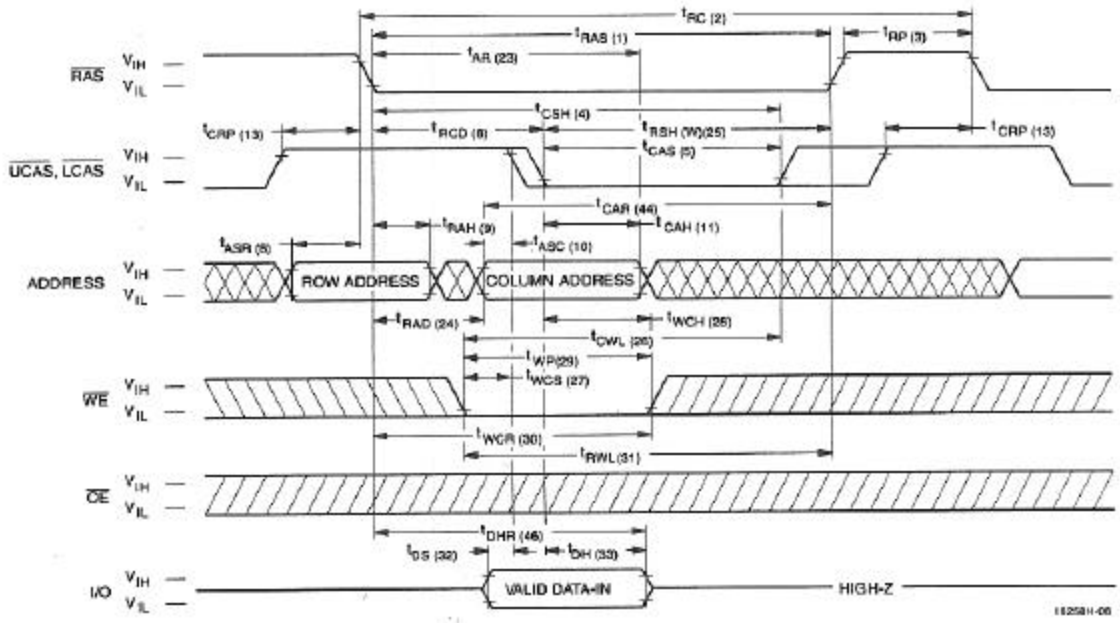
Function	RAS	LCAS	UCAS	WE	OE	ADDRESS	I/O	Notes
Standby	H	H	H	X	X	X	High-Z	
Read: Word	L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte	L	L	H	H	L	ROW/COL	Lower Byte, Data-Out Upper Byte, High-Z	
Read: Upper Byte	L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, Data-Out	
Write: Word (Early-Write)	L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)	L	L	H	L	X	ROW/COL	Lower Byte, Data-In Upper Byte, High-Z	
Read: Upper Byte (Early)	L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, Data-In	
Read-Write	L	L	L	H→L	L→H	ROW/COL	Data-Out, Data-In	1, 2
EDO Page-Mode Read	L	H→L	H→L	H	L	COL	Data-Out	2
EDO Page-Mode Write	L	H→L	H→L	L	X	COL	Data-In	2
EDO Page-Mode Read-Write	L	H→L	H→L	H→L	L→H	COL	Data-Out, Data-In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	2
CBR Refresh	H→L	L	L	X	X	X	High-Z	3
Self Refresh	H→L	L	H	X	X	X	High-Z	

Notes:
1. Byte Write cycles LCAS or UCAS active.
2. Byte Read cycles LCAS or UCAS active.
3. Only one of the two CAS must be active (LCAS or UCAS).

Waveforms of Read Cycle

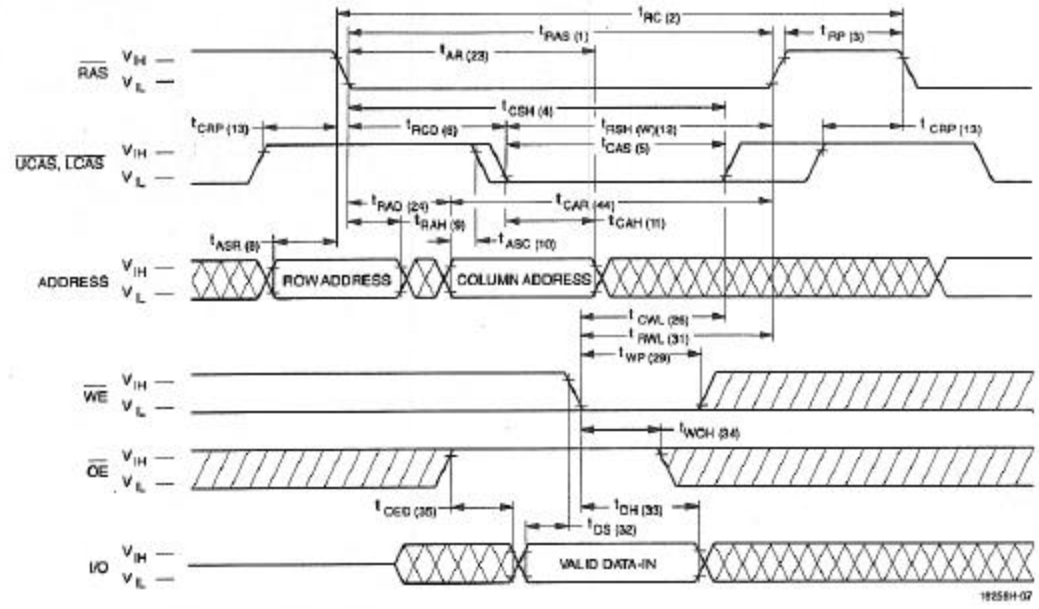


Waveforms of Early Write Cycle

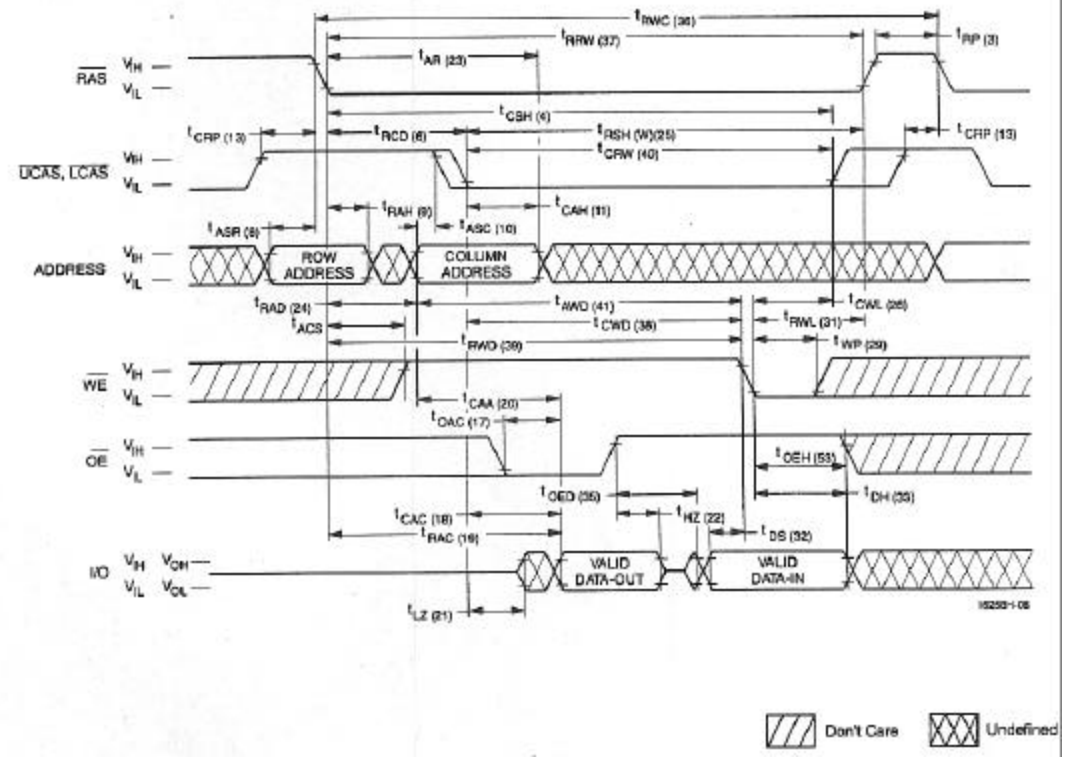


Don't Care Undefined

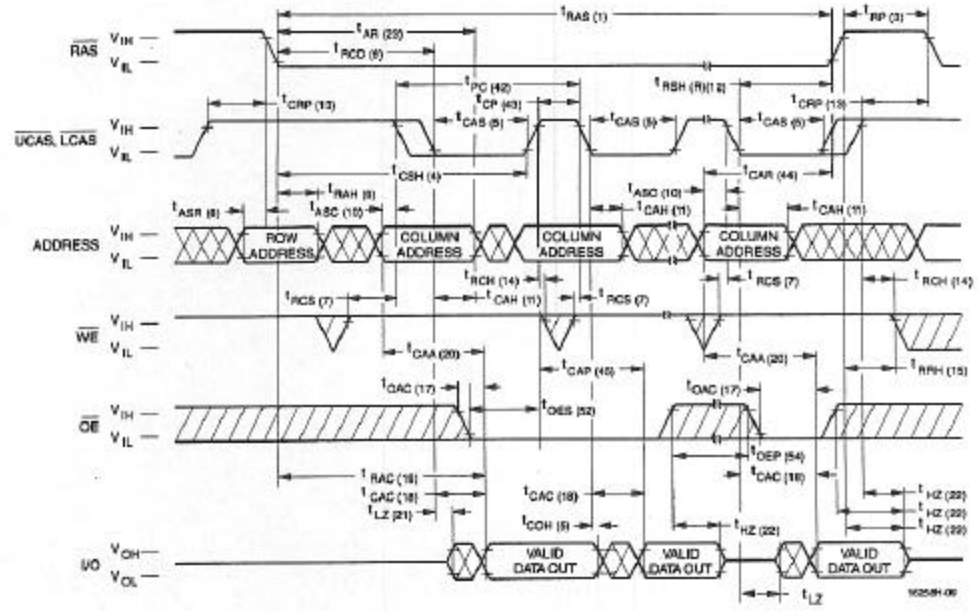
Waveforms of $\overline{OE}$-Controlled Write Cycle



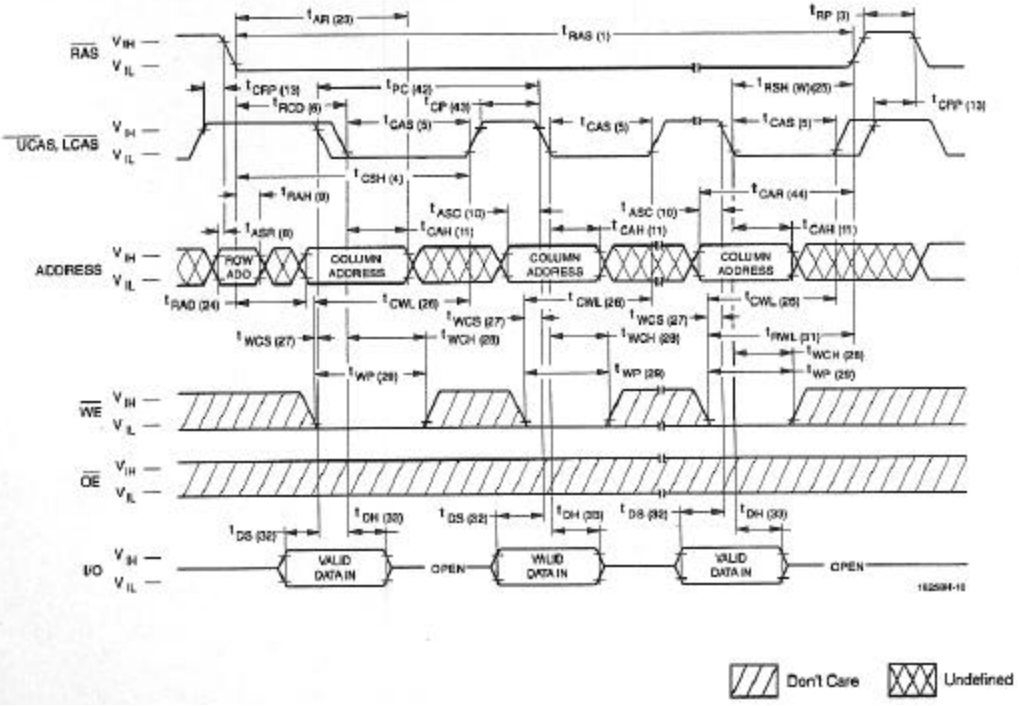
Waveforms of Read-Modify-Write Cycle



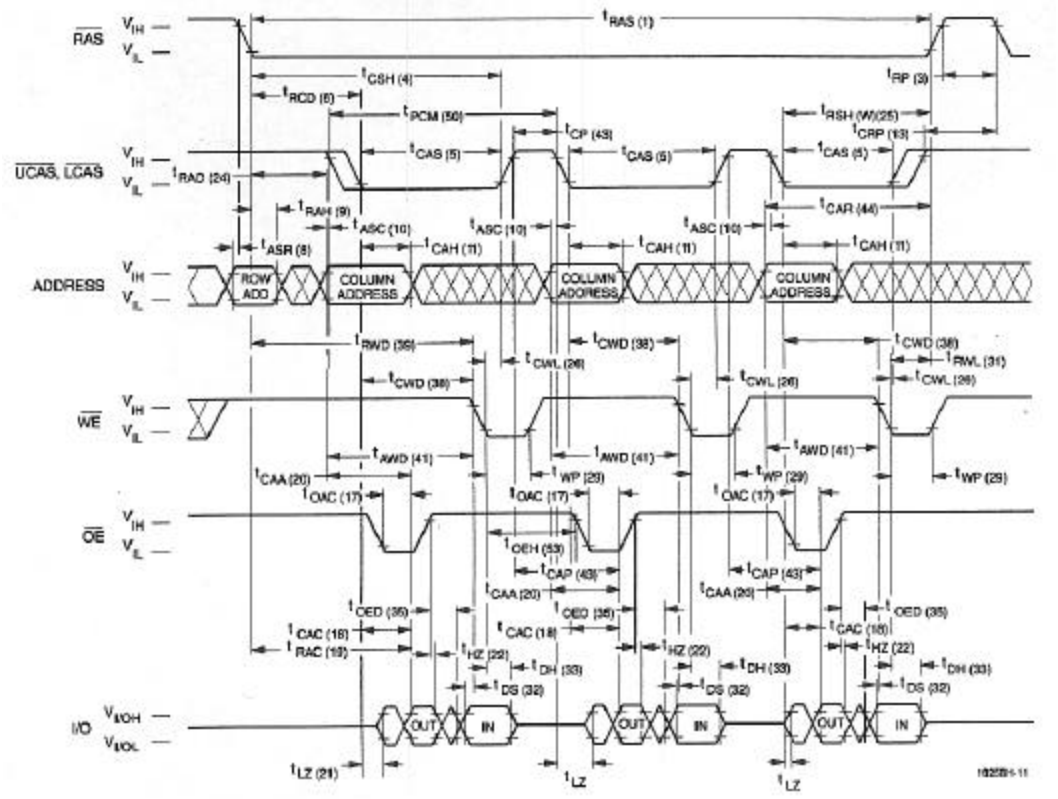
Waveforms of EDO Page Mode Read Cycle



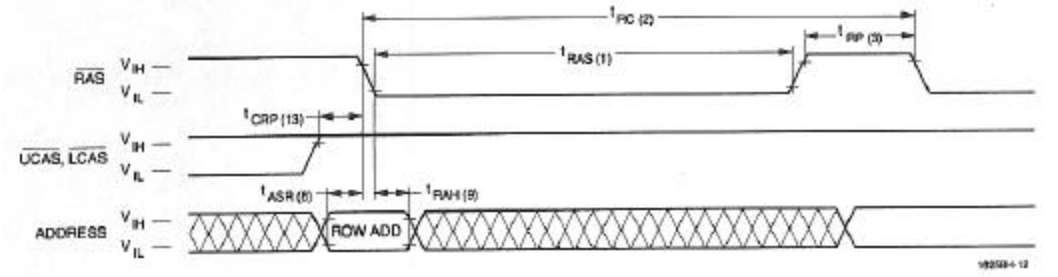
Waveforms of EDO Page Mode Write Cycle



Waveforms of EDO Page Mode Read-Write Cycle



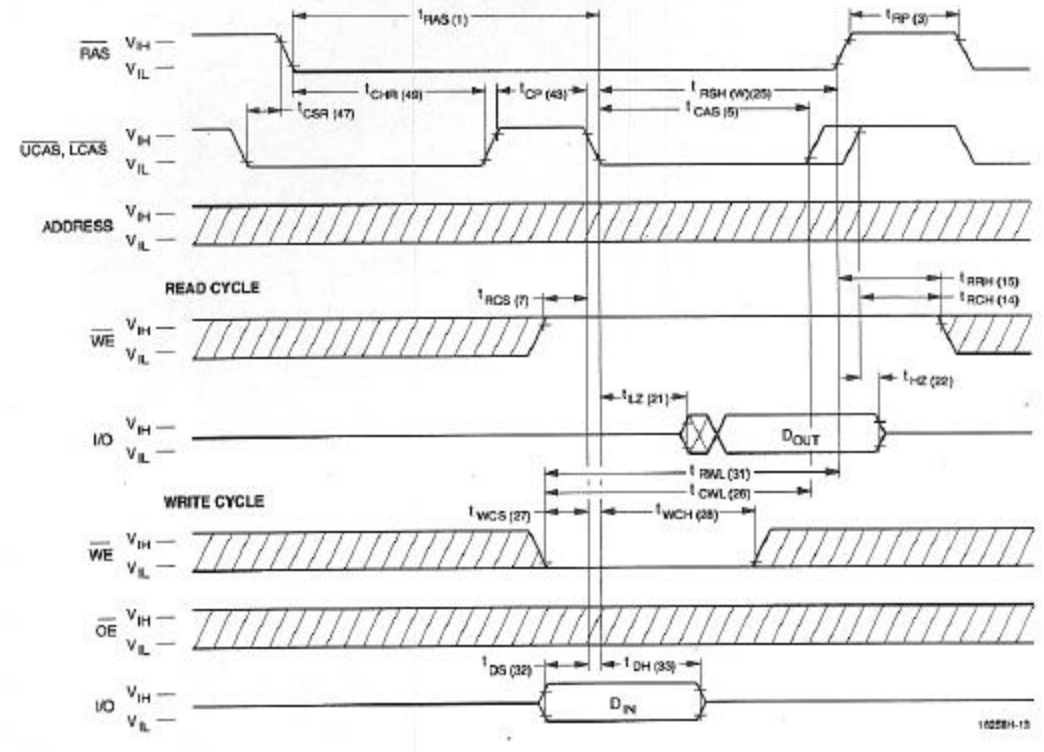
Waveforms of RAS-Only Refresh Cycle



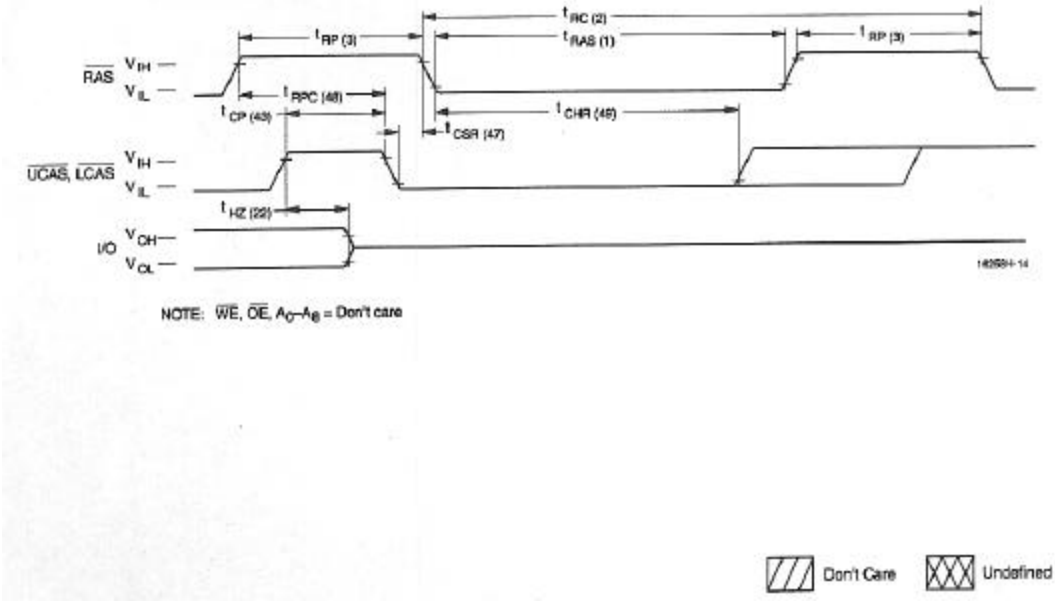
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Don't Care Undefined

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

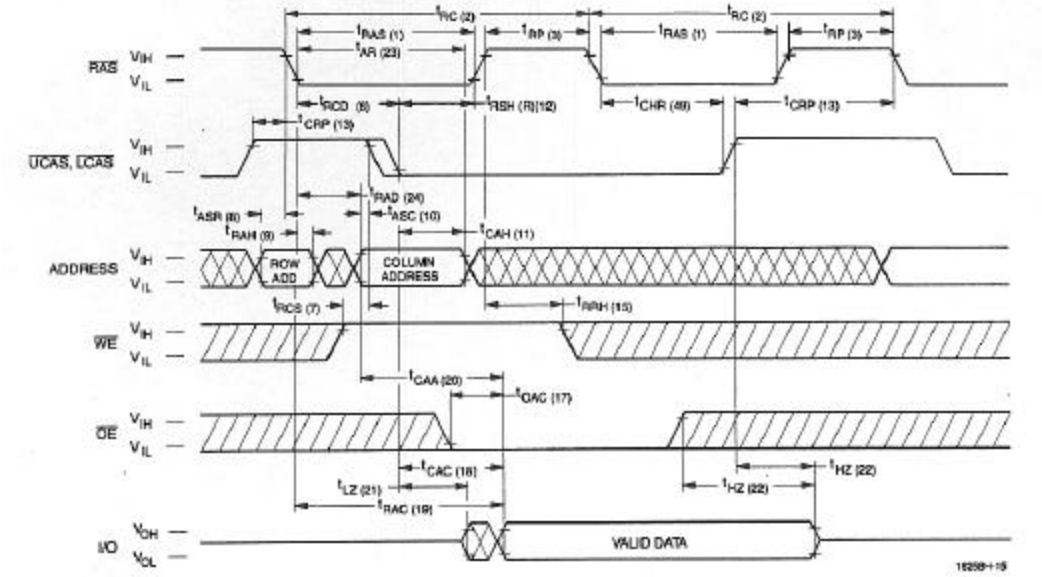


Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

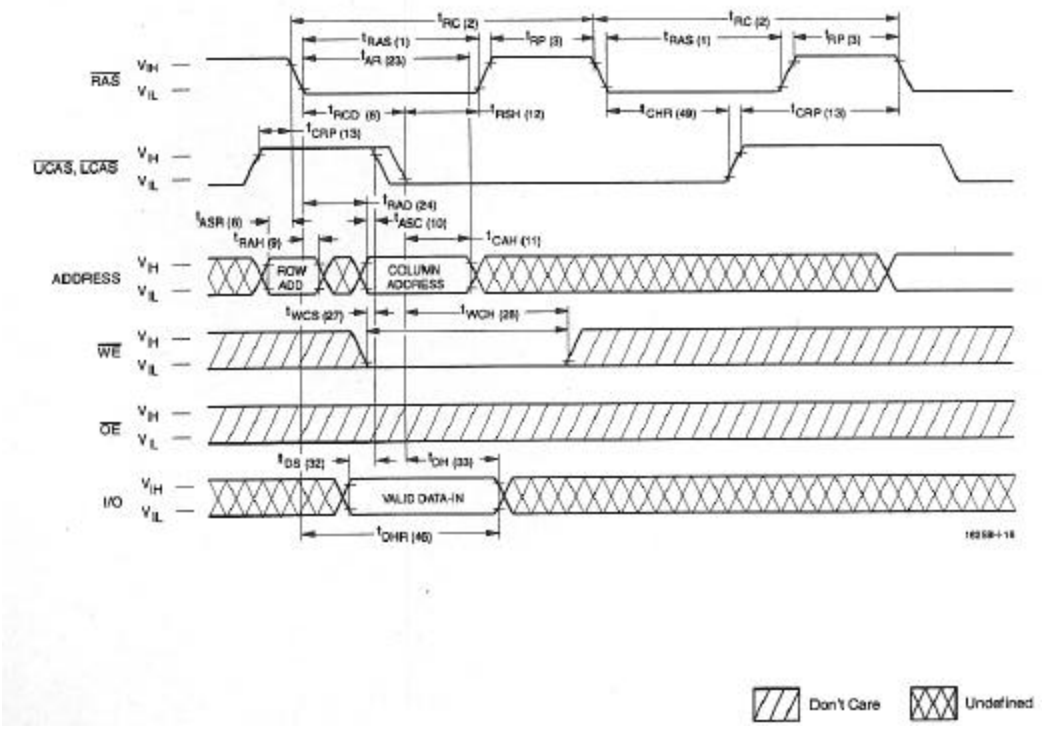


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_8 = Don't care

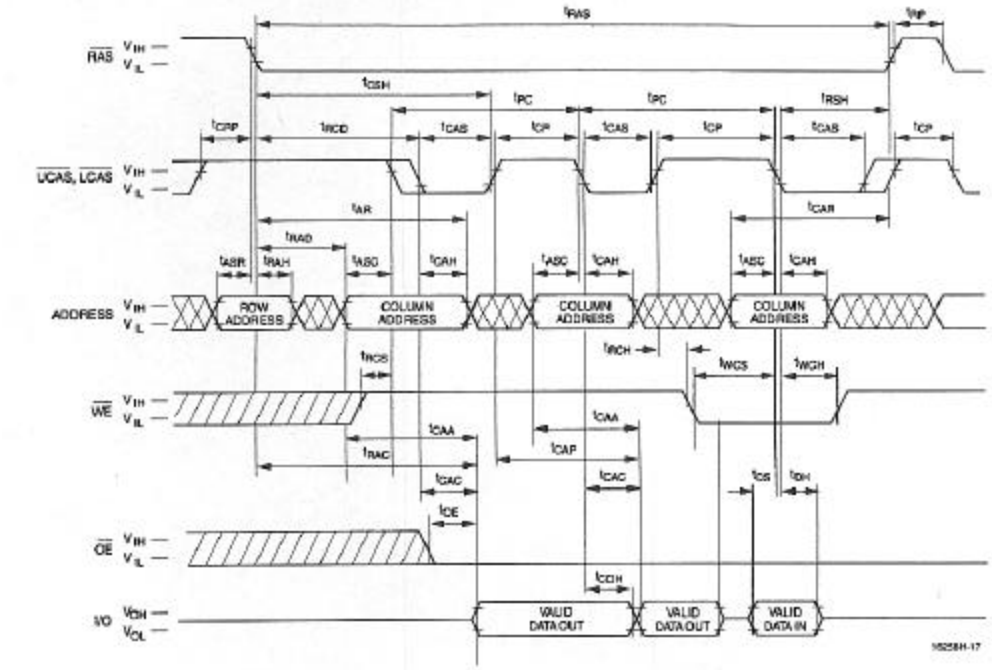
Waveforms of Hidden Refresh Cycle (Read)



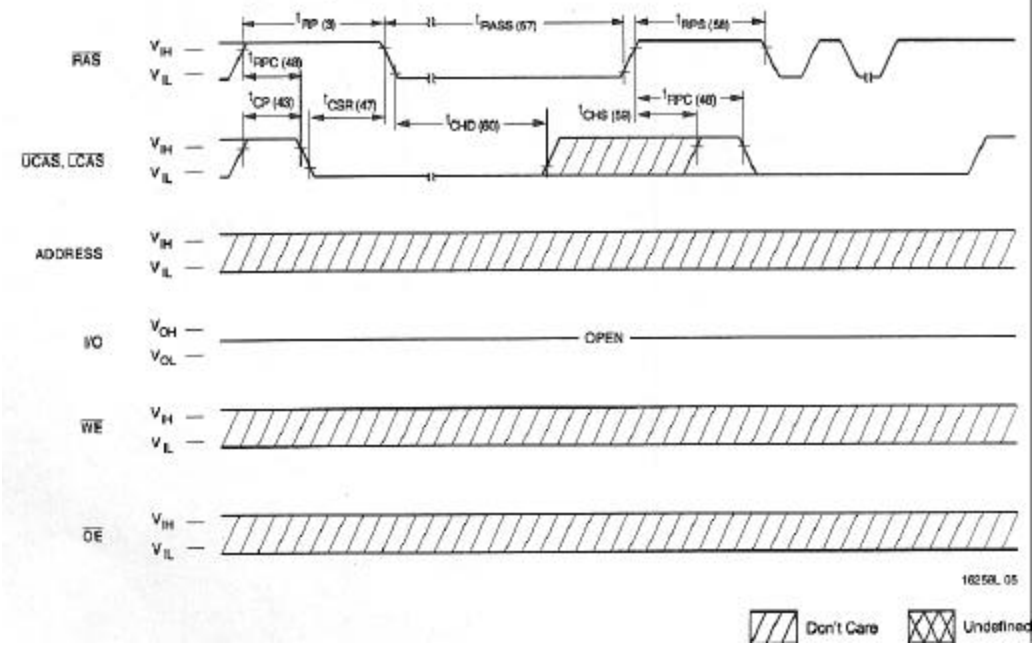
Waveforms of Hidden Refresh Cycle (Write)



Waveforms of EDO-Page-Mode Read-Early-Write Cycle (Pseudo Read-Modify-Write)



Waveforms of Self Refresh Cycle



Functional Description

The V53C16258H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C16258H reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe (RAS). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe (CAS). Because access time is primarily dependent on a valid column address rather than the precise time that the CAS edge occurs, the delay time from RAS to CAS has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing RAS low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable (WE) signal High during a RAS/CAS operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking WE and CAS low during a RAS operation. The column address is latched by CAS. The Write Cycle can be WE controlled or CAS controlled depending on whether WE or CAS falls later. Consequently, the input data must be valid at or before the falling edge of WE or CAS, whichever occurs last. In the CAS-controlled Write Cycle, when the leading edge of WE occurs prior to the CAS low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with RAS or CAS will maintain the output in the High-Z state.

In the WE controlled Write Cycle, OE must be in the high state and t_{OED} must be satisfied.

Extended Data Output Page Mode

EDO Page operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining RAS low while performing successive CAS cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while CAS is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of CAS, eliminating t_{ASC} and t_T from the critical timing path. CAS latches the address into the column address buffer. During EDO operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Hyper Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of CAS, the access time is referenced to the CAS rising edge and is specified by t_{CAP}. If the column address is valid after the rising CAS edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of CAS latches the address and enables the output.

EDO provides a sustained data rate of 83 MHz for applications that require high bandwidth such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Self Refresh

Self Refresh mode provides internal refresh control signals to the DRAM during extended periods of inactivity. Device operation in this mode provides additional power savings and design ease by elimination of external refresh control signals. Self Refresh mode is initiated with a CAS before RAS (CBR) Refresh cycle, holding both RAS low (t_{RASS}) and CAS low (t_{CHD}) for a specified period. Both of these parameters are specified with minimum values to guarantee entry into Self Refresh operation. Once the device has been placed in to Self Refresh mode the CAS clock is no longer required to maintain Self Refresh operation.

The Self Refresh mode is terminated by returning the RAS clock to a high level for a specified (t_{RPS}) minimum time. After termination of the Self Refresh cycle normal accesses to the device may be initiated immediately, providing that subsequent refresh cycles utilize the CAS before RAS (CBR) mode of operation.

Data Output Operation

The V53C16258H Input/Output is controlled by OE, CAS, WE and RAS. A RAS low transition enables the transfer of data to and from the selected row address in the Memory Array. A RAS high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a RAS low transition, a CAS low transition or CAS low level enables the internal I/O path. A CAS high transition or a CAS high level disables the I/O path and the output driver if it is enabled. A CAS low transition while RAS is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding OE high. The OE signal has no effect on any data stored in the output latches. A WE low level can also disable the output drivers when CAS is low. During a Write cycle, if WE goes low at a time in relationship to CAS that would normally cause the outputs to be active, it is necessary to use OE to disable the output drivers prior to the WE low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{CC} supply, an initial pause of 200 ìs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a RAS clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

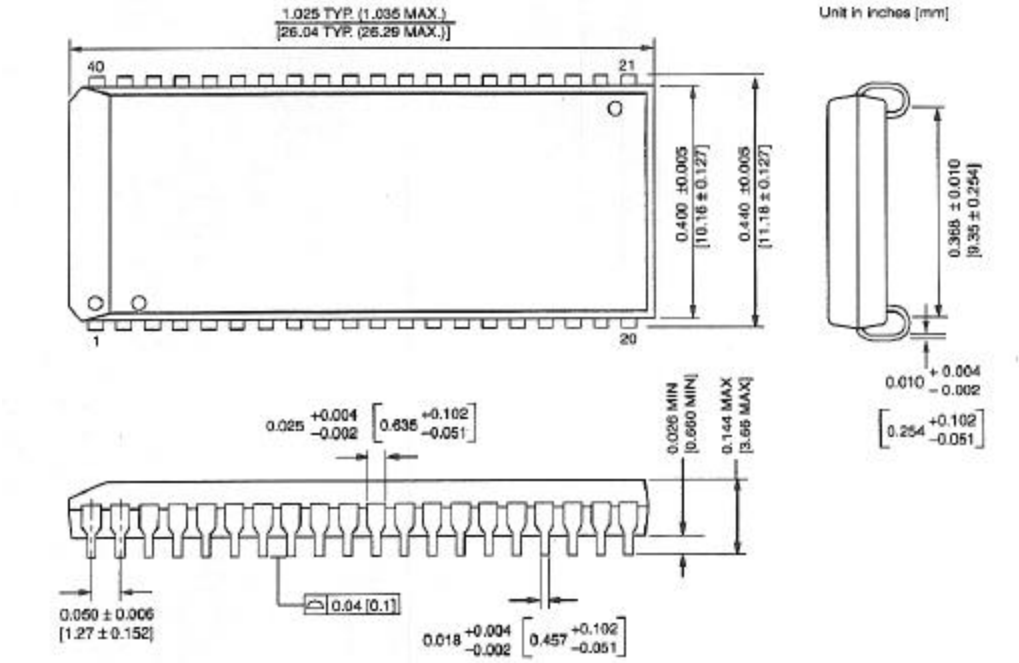
During Power-On, the V_{CC} current requirement of the V53C16258H is dependent on the input levels of RAS and CAS. If RAS is low during Power-On, the device will go into an active cycle and I_{CC} will exhibit current transients. It is recommended that RAS and CAS track with V_{CC} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C16258H Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
CAS-Controlled Write Cycle (Early Write)	High-Z
WE-Controlled Write Cycle (Late Write)	OE Controlled. High OE = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
EDO Read Cycle	Data from Addressed Memory Cell
EDO Write Cycle (Early Write)	High-Z
EDO Read-Modify-Write Cycle	Data from Addressed Memory Cell
RAS-only Refresh	High-Z
CAS-before-RAS Refresh Cycle	Data remains as in previous cycle
CAS-only Cycles	High-Z

Package Outlines

40-Pin Plastic SOJ



40/44L-Pin TSOP-II